CLAIMS

What is claimed is:

1. A runtime repairable processor within a single silicon chip, comprising:

a plurality of data registers;

a first computing unit;

an area of the silicon chip defined by at most a plurality of data paths for connecting the plurality of data registers to the first computing unit; and

a second computing unit, wherein the second computing unit is a duplicate of the first computing unit and is connected to the plurality of data registers, the first computing unit and the second computing unit being placed within the area.

2. The runtime repairable processor of claim 1, further comprising an enabling control logic, wherein the enabling control logic disables the first computing unit and enables the second computing unit when a failure is detected with the first computing unit.

3. The runtime repairable processor of claim 2, wherein the enabling control logic enables a computing unit by enabling a clock signal to that computing unit.

4. The runtime repairable processor of claim 2, further comprising a machine state register including a unit selecting indicator, the unit selecting indicator controlling the enabling control logic.

5. The runtime repairable processor of claim 4, wherein the unit selecting indicator is set by software.

6. The runtime repairable processor of claim 1, wherein the first computing unit further comprises a first error indicator and the second computing unit further comprises a second error indicator.

7. The runtime repairable processor of claim 6, further comprising a machine check trap wherein the first and second error indicators are stored, the machine check trap being used to initiate a software diagnostic routine.

8. The runtime repairable processor of claim 1, wherein the first computing unit is an adder.

9. The runtime repairable processor of claim 1, wherein the first computing unit is a rotator.

10. The runtime repairable processor of claim 1, wherein the first computing unit is an arithmetic logic unit.

11. A method for providing a fault tolerant computing through a single chip runtime repairable processor, comprising the steps of:

connecting a plurality of data registers to a first computing unit through a plurality of data paths;

defining an area of the chip that covers at most the plurality of the data paths, wherein the first computing unit and the plurality of data registers are confined within the area;

placing a second computing unit within the area, wherein the second computing unit being a duplicate of the first computing unit;

connecting the plurality of data registers to the second computing unit;

detecting an error condition in the first computing unit;

in response to detecting the error condition, disabling the first computing unit; and

in response to disabling the first computing unit, enabling the second computing unit.

12. The method of claim 11, wherein the disabling step and the enabling step are controlled by a machine state register.

13. The method of claim 11, further comprising the step of, in response to detecting an error condition, setting a unit swapping indicator in a machine state register.

14. The method of claim 11, further comprising the step of, in response to detecting an error condition, executing a diagnostic procedure.

15. The method of claim 11, wherein the step of disabling the first computing unit further comprises the step of disabling a clock signal to the first computing unit.

16. The method of claim 11, wherein the step of enabling the second computing unit further comprises the step of enabling a clock signal to the second computing unit.

17. The method of claim 11, further comprising the steps of:

trapping the error condition in a machine check trap; and

in response to trapping the error condition, causing a diagnostic routine to run on the first computing unit.

18. A runtime repairable processor within a single silicon chip, comprising:

means for storing data;

a first computing means for performing computations;

means for devising a plurality of data paths for connecting the means for storing data to the first computing means; and

a second computing means for performing computations, wherein the second computing means is a duplicate of the first computing means and is connected to the means for storing data, the first computing means and the second computing means being placed within the area defined by at most the means for devising a plurality of data paths.